What is claimed is:

1. An MRAM comprising:

a semiconductor substrate;

a transistor formed on the semiconductor substrate;

an interlayer dielectric formed on the semiconductor substrate to cover the transistor; and

first and second MTJ cells formed in the interlayer dielectric to be coupled in parallel with a drain region of the transistor,

wherein the first MTJ cell is coupled to a first bit line formed in the interlayer dielectric and the second MTJ cell is coupled to a second bit line formed in the interlayer dielectric,

and wherein a data line is formed between the first MTJ cell and a gate electrode of the transistor to be perpendicular to the first bit line and the second bit line.

2. The MRAM as claimed in claim 1, further comprising a pad conductive layer disposed between the first MTJ cell and the data line to be coupled to the drain region, wherein the first MTJ cell and the second MTJ cell are formed on the pad conductive layer.

3. The MRAM as claimed in claim 2, further comprising a dummy data line formed below the pad conductive layer in a region in which the second MTJ cell is formed.

4. The MRAM as claimed in claim 2, further comprising:

a contact hole formed in the interlayer dielectric to expose a portion of the drain region; and

a conductive plug filling the contact hole,

wherein the pad conductive layer contacts an entire exposed surface of the conductive plug filling the contact hole.

5. The MRAM as claimed in claim 2, wherein the interlayer dielectric comprises a first interlayer dielectric covering the transistor, a second interlayer dielectric formed on the first interlayer dielectric to cover the data line, and a third interlayer dielectric formed between the first and second bit lines and the second interlayer dielectric to surround the pad conductive layer, which is formed on the second interlayer dielectric, and the first and second MTJ cells, which are stacked on the pad conductive layer.

6. The MRAM as claimed in claim 5, further comprising a second contact hole and a third contact hole formed in the third interlayer dielectric

to expose predetermined portions of the first MTJ cell and the second MTJ cell, respectively.

7. The MRAM as claimed in claim 6, wherein the first bit line is formed on the third interlayer dielectric to be coupled to the first MTJ cell through the second contact hole.

8. The MRAM as claimed in claim 6, wherein the second bit line is formed on the third interlayer dielectric to be coupled to the second MTJ cell through the third contact hole.

9. The MRAM as claimed in claim 1, wherein the first MTJ cell is a main cell and the second MTJ cell is a reference cell.

10. A method for fabricating an MRAM, comprising:

(1) forming a transistor on a semiconductor substrate;

(2) forming a first interlayer dielectric on the semiconductor substrate to cover the transistor;

(3) forming a first data line on the first interlayer dielectric;

(4) forming a second interlayer dielectric on the first interlayer dielectric to cover the first data line;

(5) forming a pad conductive layer on a portion of the second interlayer dielectric to be coupled to a drain region of the transistor, wherein the pad conductive layer is formed to be symmetric about the drain region;

(6) forming a first MTJ cell and a second MTJ cell spaced apart from the first MTJ cell on the pad conductive layer;

(7) forming a third interlayer dielectric on the second interlayer dielectric to cover the pad conductive layer, the first MTJ cell, and the second MTJ cell; and

(8) forming a first bit line coupled to the first MTJ cell and a second bit line coupled to the second MTJ cell on the third interlayer dielectric.

11. The method as claimed in claim 10, wherein forming the pad conductive layer on the portion of the second interlayer dielectric to be coupled to a drain region of the transistor further comprises:

forming a first contact hole in the first interlayer dielectric and the second interlayer dielectric to be spaced apart from the first data line and to expose a portion of the drain region of the transistor; and

forming the pad conductive layer on the portion of the second interlayer dielectric to fill the first contact hole.

12. The method as claimed in claim 10, wherein forming the pad conductive layer on the portion of the second interlayer dielectric to be coupled to a drain region of the transistor further comprises:

forming a first contact hole in the first interlayer dielectric and the second interlayer dielectric to be spaced apart from the first data line and to expose a portion of the drain region of the transistor;

filling the first contact hole with a conductive plug; and

forming the pad conductive layer on the portion of the second interlayer dielectric to contact an entire exposed surface of the conductive plug.

13. The method as claimed in claim 10, wherein forming the first data line on the first interlayer dielectric further comprises simultaneously forming a dummy data line on the first interlayer dielectric to be spaced apart from the first data line.

14. The method as claimed in claim 10, wherein forming the first bit line coupled to the first MTJ cell and the second bit line coupled to the second MTJ cell on the third interlayer dielectric further comprises:

forming a second contact hole and a third contact hole in the third interlayer dielectric to expose a portion of the first MTJ cell and a portion of the second MTJ cell, respectively; and

simultaneously forming the first bit line filling the second contact hole and the second bit line filling the third contact hole on the third interlayer dielectric.